UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/611,395	06/30/2003	Shriram Ramanathan	42P16666	1525

8791 7590 10/03/2007

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040

EXAMINER	
RODGERS, COLLEEN E	

ART UNIT	PAPER NUMBER
2813	

MAIL DATE	DELIVERY MODE
10/03/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

T4

Office Action Summary	Application No.	Applicant(s)	
	10/611,395	RAMANATHAN ET AL.	
	Examiner	Art Unit	
	Colleen E. Rodgers	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 July 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-20 and 22-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-20 and 22-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action responds to the Amendment filed 17 July 2007. By this amendment, claims 1, 12, 13 and 27 are amended and claims 6, 21 and 28-42 are canceled. Claims 1-5, 7-20 and 22-27 remain pending.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 2, 4, 5, 8, 10, 11, 13, 14, 16-20, 23, 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Kellar et al** (US Patent Application Publication 2003/0157782).

Regarding claims 1 and 13, **Kellar et al** disclose a method comprising:

depositing a layer of metal **106** on each of a number of conductors **224** disposed on a surface of a first wafer **222**;

aligning the first wafer with a second wafer **212**, the second wafer having a number of conductors **106** disclosed on the surface thereof;

physically contacting the metal layer on each of the conductors of the first wafer with a mating one of the conductors on the second wafer [see Fig. 2]; and

forming a bond between the metal layer on each of the conductors of the first wafer and the mating one conductor of the second wafer, wherein all regions of the first and second wafer surfaces surrounding the mating conductors remain unbonded [see paragraph 0024].

Kellar et al are silent as to the temperature at which the bond is formed. However, these claims are *prima facie* obvious without a showing that the claimed ranges achieve unexpected results relative to the prior art range. *In re Woodruff*, 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also *In re Huang*, 40 USPQ2d 1685, 1688 (Fed. Cir. 1996) (claimed ranges of a result effective variable, which do not overlap the prior art ranges, are unpatentable unless they produce a new and unexpected result which is different in kind and not merely in degree from the results of the prior art). See also *In re Boesch*, 205 USPQ 215 (CCPA) (discovery of optimum value of result effective variable in known process is ordinarily within skill of art) and *In re Aller*, 105 USPQ 233 (CCPA 1955) (selection of optimum ranges within prior art in general conditions is obvious). In this case, there exists no evidence of record that the temperature at which the bond is formed provides unexpected results in the bond produced. One of ordinary skill in the art would be motivated to optimize the bonding temperature to provide for processing limitations, including the reflow temperatures of the materials used.

Regarding claims 2 and 14, **Kellar et al** disclose the method of claims 1 and 13, respectively, furthermore wherein, prior to depositing the metal layer on each of the conductors of the first wafer, removing dielectric material from the surface of the first wafer [see paragraph 0027, wherein a dielectric recess is formed].

Regarding claim 4, **Kellar et al** disclose the method of claim 1, furthermore wherein the conductors of the first wafer comprise copper [see paragraph 0024].

Regarding claim 5, **Kellar et al** disclose the method of claim 1, furthermore wherein the metal comprises a metal selected from the group consisting of silver, gold or palladium [see paragraph 0024].

Regarding claims 8 and 23, **Kellar et al** disclose the method of claims 1 and 13, respectively, furthermore wherein depositing the layer of metal on each of the conductors of the first wafer comprises selectively depositing the metal on each of the conductors [see paragraphs 0027-0028].

Regarding claims 10 and 25, **Kellar et al** disclose the method of claims 1 and 13, respectively, furthermore wherein the metal layer **106** on each of the conductors **224** of the first wafer comprises a number of islands [see Fig. 2].

Regarding claims 11 and 26, **Kellar et al** disclose the method of claims 10 and 25, respectively, furthermore wherein the islands are selectively deposited on each of the conductors of the first wafer [see paragraphs 0027-0028].

Regarding claims 16-20, **Kellar et al** disclose the method of claim 13, furthermore wherein the conductors and the metal of each of the first and second wafers comprise the same metal, specifically copper, or different materials, including silver, gold or palladium [see paragraph 0024].

4. Claims 3 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Kellar et al** (US Patent Application Publication 2003/0157782) in view of **Tong et al** (US Patent Application Publication 2004/0157407).

Regarding claims 3 and 15, **Kellar et al** disclose the method of claims 1 and 13, respectively. **Kellar et al** do not teach that, prior to depositing the metal layer on each of the conductors of the first wafer, native oxide must be removed from the conductors. **Tong et al** teach a method of bonding in a similar manner, including the same materials (namely, copper). Furthermore, **Tong et al** teach that sputter cleaning and evaporation are employed to remove native oxide [see paragraph 0075]. It would have been obvious to one of ordinary skill in the art at the time of invention to

clean native oxide from the surfaces of the metals to be bonded in order to reduce the contact resistance.

5. Claims 7, 12, 22 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Kellar et al** (US Patent Application Publication 2003/0157782) in view of **Mirkin et al** (US Patent Application Publication 2004/0226464).

Regarding claims 7 and 22, **Kellar et al** disclose the method of claims 1 and 13, respectively. **Kellar et al** do not disclose wherein depositing the layer of metal on each of the conductors of the first wafer comprises forming a blanket layer of the metal over the conductors and the surface of the first wafer and removing the metal from at least portions of the first wafer surface. **Mirkin et al** teach a method of bonding wafers, wherein a metal layer **132** is formed over a conductor **126** on a first wafer **120**. Furthermore, **Mirkin et al** teach wherein the metal layer is formed by forming a blanket layer of material and removing the metal from at least portions of the first wafer surfaces [see paragraph 0044]. It would have been obvious to one of ordinary skill in the art at the time of invention to use the method of **Mirkin et al** in the process taught by **Kellar et al** because it is well known in the art to form a blanket layer and pattern it in order to arrive at an island configuration.

Regarding claims 12 and 27, **Kellar et al** disclose a method comprising:

depositing a layer of metal **106** on each of a number of conductors **224** disposed on a surface of a first wafer **222**;

aligning the first wafer with a second wafer **212**, the second wafer having a number of conductors **106** disclosed on the surface thereof;

physically contacting the metal layer on each of the conductors of the first wafer with a mating one of the conductors on the second wafer [see Fig. 2]; and

forming a bond between the metal layer on each of the conductors of the first wafer and the mating one conductor of the second wafer, wherein all regions of the first and second wafer surfaces surrounding the mating conductors remain unbonded [see paragraph 0024],

wherein the metal layer on each of the conductors of the first wafer comprises a number of islands [see Fig. 2].

Kellar et al do not disclose wherein the islands are formed by a process comprising depositing a blanket layer of the metal over the conductors and the surface of the first wafer and removing the metal from at least portions of the first wafer surface. **Mirkin et al** teach a method of bonding wafers, wherein a metal layer **132** is formed over a conductor **126** on a first wafer **120**. Furthermore, **Mirkin et al** teach wherein the metal layer is formed by forming a blanket layer of material and removing the metal from at least portions of the first wafer surfaces [see paragraph 0044]. It would have been obvious to one of ordinary skill in the art at the time of invention to use the method of **Mirkin et al** in the process taught by **Kellar et al** because it is well known in the art to form a blanket layer and pattern it in order to arrive at an island configuration.

6. Claims 9 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Kellar et al** (US Patent Application Publication 2003/0157782) in view of **Neuhaus et al** (US Patent Application Publication 2002/0027294).

Regarding claims 9 and 24, **Kellar et al** disclose the method of claims 8 and 23, respectively. **Kellar et al** do not disclose wherein selectively depositing the metal on each of the conductors of the first wafer comprises an electroless plating process, an electroplating process, or a contact displacement process. **Neuhaus et al** disclose a method of performing metal-metal bonding for semiconductor wafers comprising electroplating a number of metallic islands to a metallized contact

[see paragraph 0027-0028, 0038 and 0073]. It would have been obvious to one of ordinary skill in the art at the time of invention to use the method of **Neuhaus et al** in the method of **Kellar et al** because **Neuhaus et al** teach that this method eliminates several manufacturing steps, which simplifies the process for component assembly. Furthermore, it proves improved electrical performance, such as lower metal-to-metal contact resistance [see paragraph 0021].

Response to Arguments

7. Applicant's arguments with respect to claims 1-5, 7-20 and 22-27 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Colleen E. Rodgers whose telephone number is (571) 272-8603. The examiner can normally be reached on Monday through Friday, 9:00 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

CER

CARL WHITEHEAD, JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800